A New Harmonics Elimination Method Applied to a Static VAR Compensator Using a Three Level Inverter

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Abstract

In this paper the use of harmonics elimination method applied to a three level inverter is shown. The method that calculates the switching angles is shown. Simulations results using PSspice program are carried out to validate the mathematical model.

Moreover, the proposed harmonics elimination method was used to control the static VAR compensator (ASVC) which uses a three level voltage source inverter.

Keywords

ASVC, PSpice, PWM, Harmonics, Three-level inverter

1. Introduction

The fast growing development of ultra rapid power switching devices and the desire to reduce the harmonics has lead to the increase in use of converters for large-scale reactive power compensation. Such an SVC is made up of two level voltage source inverter and presents a fast response time, reduced harmonic pollution. However, for very high power application and voltages these SVC's are unsuitable. Recently the multilevel pulse width

modulation (PWM) [1] converter topology has drawn tremendous interest in the power industry since it can easily provide the high power required for high power applications for such uses as static VAR compensation, active power filters, and so that large motors can also be controlled by high power adjustable frequency drives [2-5].

The most popular structure proposed as a transformer less voltage source inverter is the diode clamped converter based on the neutral point clamped (NPC) converter proposed by Nabae [1]. It has the advantages that the blocking voltage of each switching device is one half of dc link voltage and the harmonics contents output voltage is far less than those of two-level inverter at the same switching frequency.

The multilevel voltage source inverters unique structure allows them to reach high voltages with low harmonics without the use of transformers or series connected synchronized switching devices, a benefit that many contributors have been trying to appropriate for high voltage, high power applications [6-9]. It is well known that for a classical inverter voltages are generated with harmonics of the order (6K 1)f, and the input current at steady state contains frequency components equal to 6K f with f: output fundamental frequency [10-11] and K=1, 2, 3, … One of the solutions applied is the use of multilevel inverter topology. Fig. 1 shows the structure of a three level inverter used as a compensator each leg of the inverter is made up of four pairs of diode - GTO's.

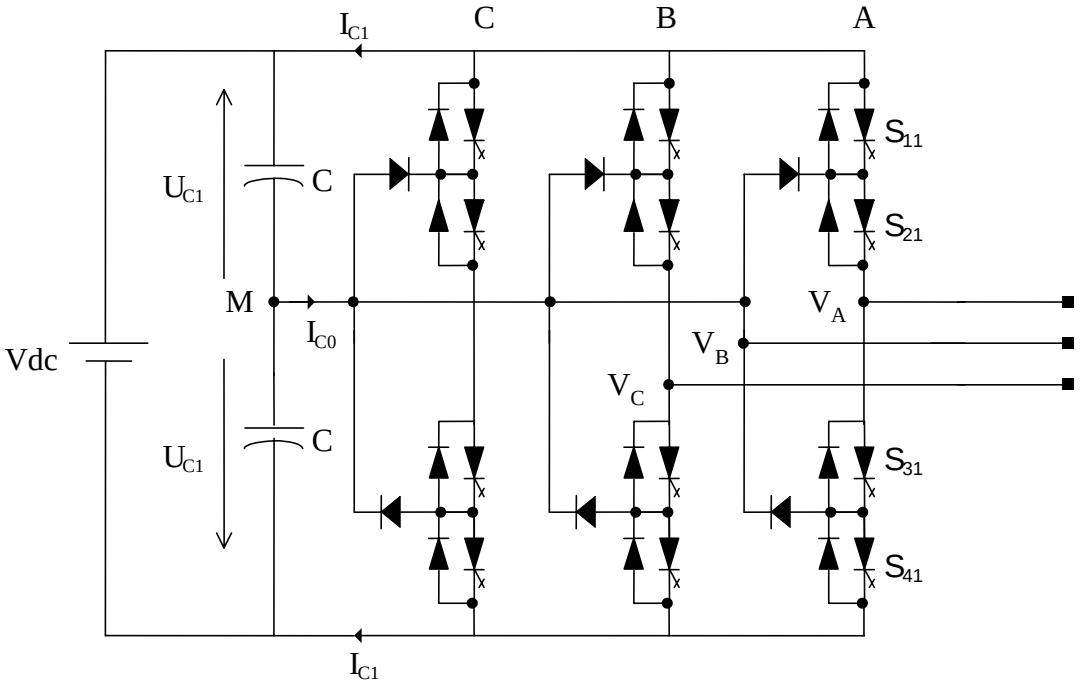

Fig.1. Topology of a three level inverter

Each represents a bi-directional switch and two auxiliary diodes allowing having zero voltage at the output of the inverter. The system obtained is connected to an RL load, the DC side is composed of two capacitors behaving as a voltage divider supplied from a DC source [13].

2. PWM control for harmonics elimination

The switching angles are either fixed by the intersection of a reference wave and a modulating signal, PWM case, or full wave control. A third alternative control method is possible when we use a system controlled by microprocessor for the switching through the pre-calculated sequences and then stored in a memory [14].

The determination of the control angles may then be carried out based on complex criteria, since the angles have already been calculated. The performances of the system depend on the choice of the criteria used for calculating the angles; it is interesting to note that any method used will consist always on eliminating the effect obtained by the presence of harmonics on the output voltage of the inverter.

Fig. 2 shows the control signals of the four switches of one leg of the three phase three level inverter and the phase voltage to the neutral point M. The pulses given in fig. 2a and fig. 2b control the switches S_{11} and S_{21}. The complementary pulses to S_{11} and S_{21} respectively in fig. 2c and fig. 2d control the switches S_{13} and S_{14}. The voltage between a phase and neutral point M is illustrated by fig. 2e we notice that the voltage V_{AM} is symmetrical with respect to M. Fourier coefficients for such a signal V_{AM} are given by:

$$a_r = \frac{4}{r\pi}\left[\sum_{j=1}^{R}(-1)^{j+1}\cos\left(r\alpha_j\right)\right] \qquad (1)$$

with R the harmonics range (1,2…R).

These equations are non linear, and multiple solutions are possible. But all the solutions of equation (1) must satisfy the following constraint:

$$\alpha_1 \langle \alpha_2 \langle \alpha_3 \langle \ldots\ldots \langle \alpha_R \langle \frac{\pi}{2} \qquad (2)$$

The non-linear equations to eliminate R-1 harmonics non multiple of three such as 5,7,11, etc. are written as follows:

$$\begin{bmatrix} \cos\alpha_1 & -\cos\alpha_2 & \ldots\ldots\ldots & (-1)^{j+1}\cos\alpha_j \\ \cos 5\alpha_1 & -\cos 5\alpha_2 & \ldots\ldots\ldots & (-1)^{j+1}\cos 5\alpha_j \\ . & . & . & . \\ . & . & . & . \\ \cos x\alpha_1 & \cos x\alpha_2 & \ldots\ldots\ldots & (-1)^{j+1}\cos x\alpha_j \end{bmatrix} = \begin{bmatrix} \frac{\pi\ a_1}{4} \\ 1 \\ . \\ . \\ 1 \end{bmatrix} \quad (3)$$

with x = 3R-1 for R even, and x = 3R-2 for R odd.

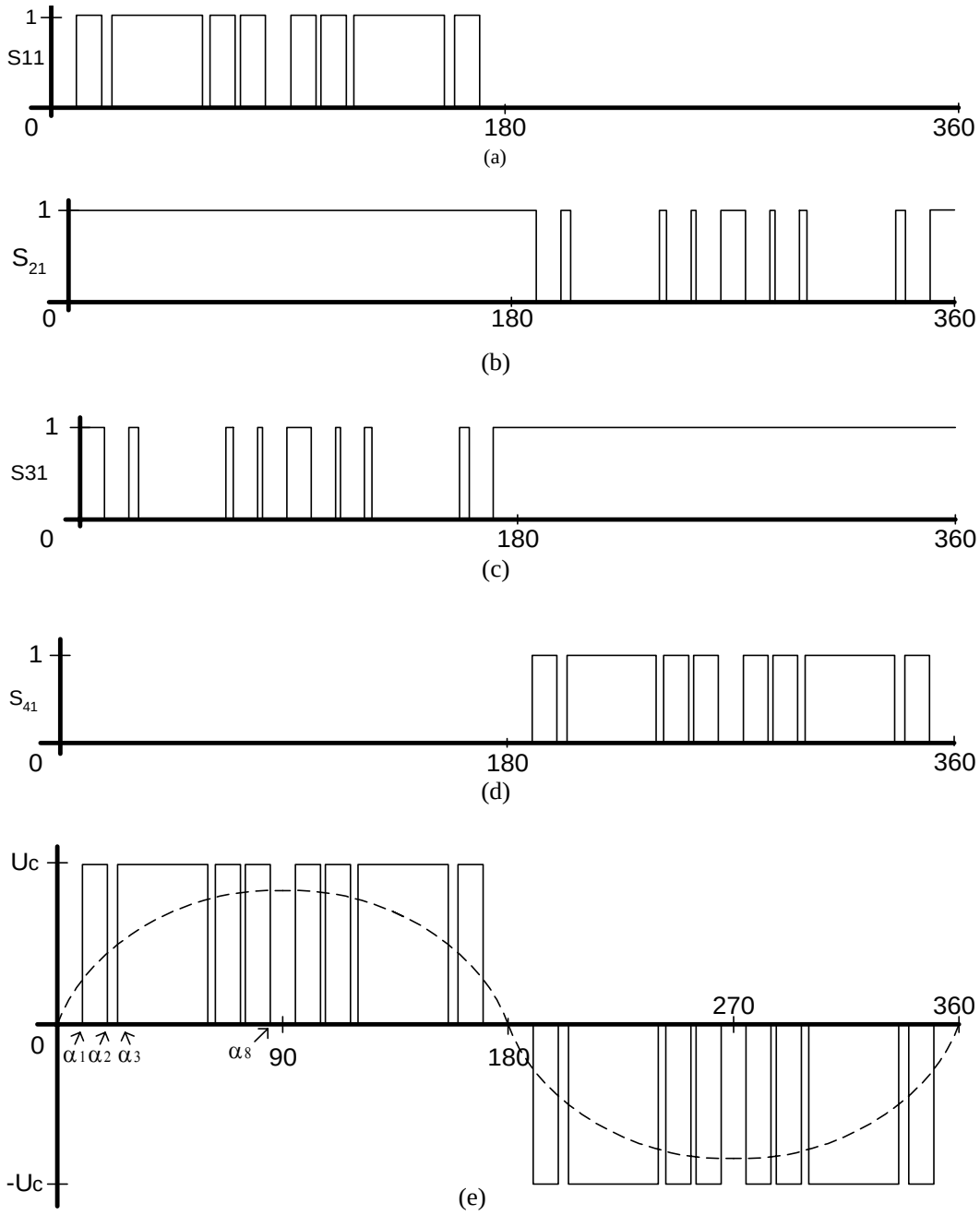

Fig. 2. Voltage between and point M VAM and the pulses for one leg of the inverter for (R=8) (a) pulses for S_{11}; (b) pulses for S_{21}; (c) pulses for S_{31}; (d) pulses for S_{41}; (e)Voltage V_{AM}

To solve the system of equation (3) we use Newton Raphson method, using a program MATLAB program [2]. Fig. 3 shows the trajectory of the solutions for various values of R, with modulation index "MI" varying in the interval [0 1.1].

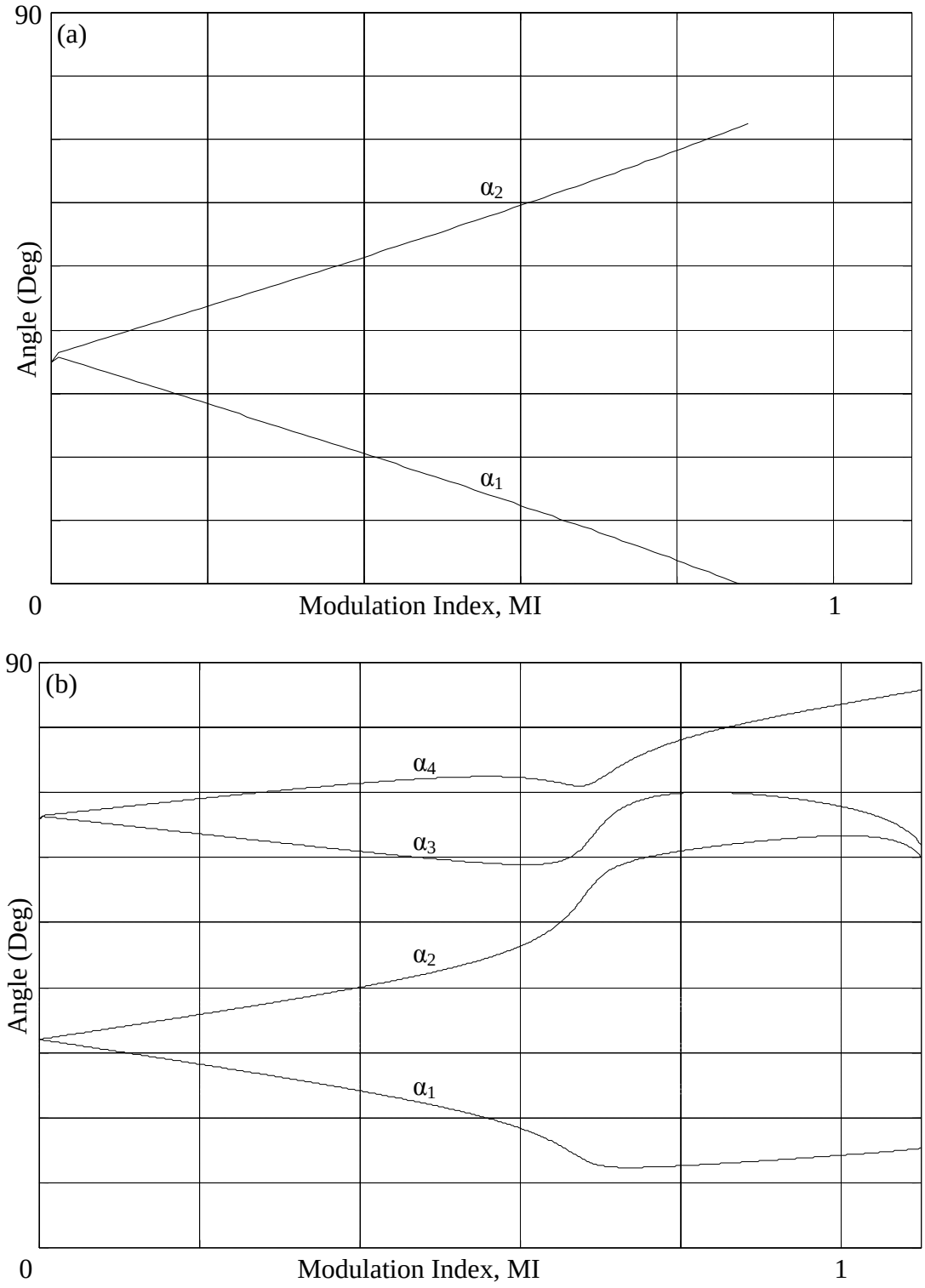

Fig. 3. Trajectories of Solutions for programmed PWM: (a) R = 2, and (b) R = 4

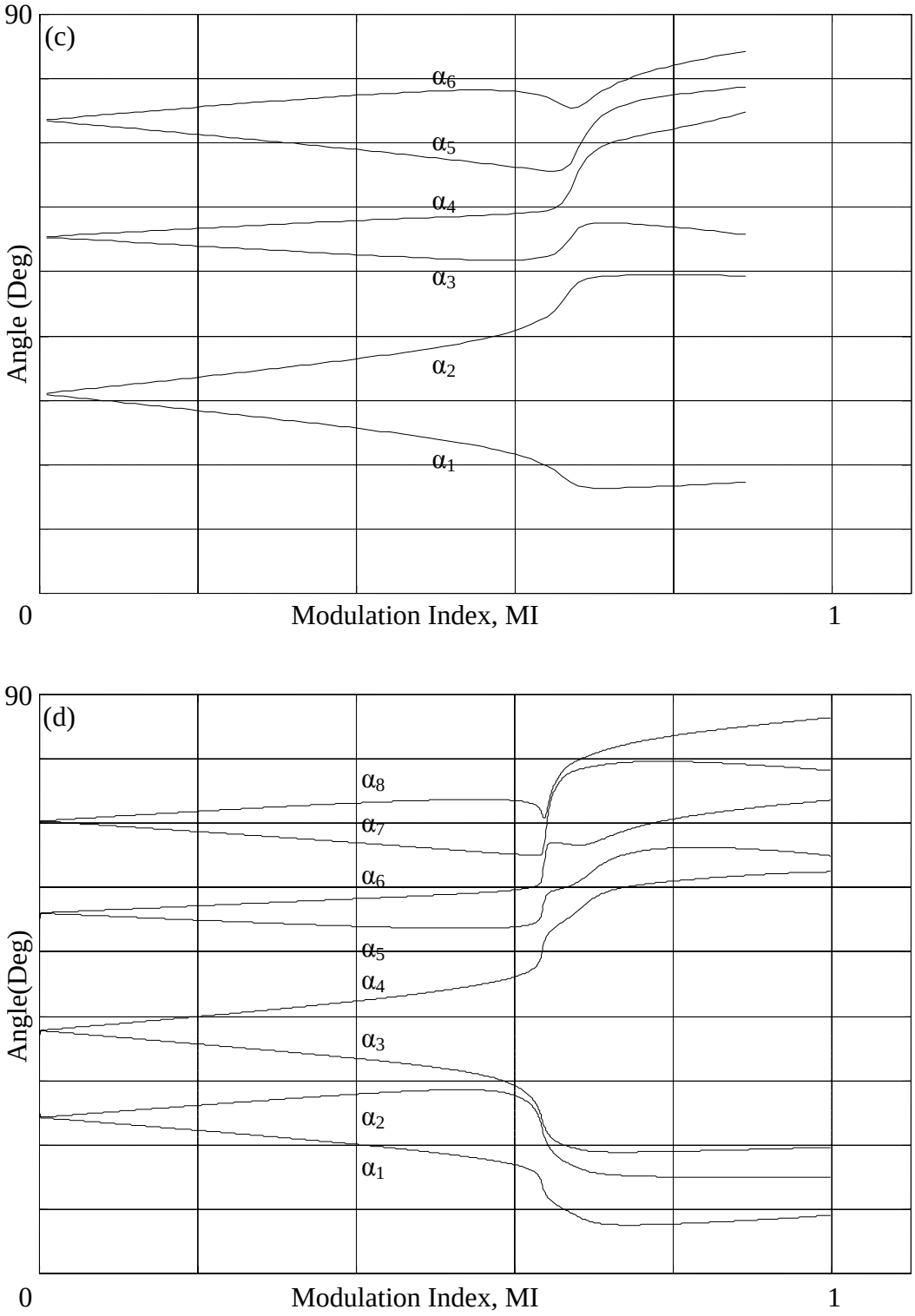

Fig. 3. Trajectories of Solutions for programmed PWM: (c) R = 6, and (d) R=8

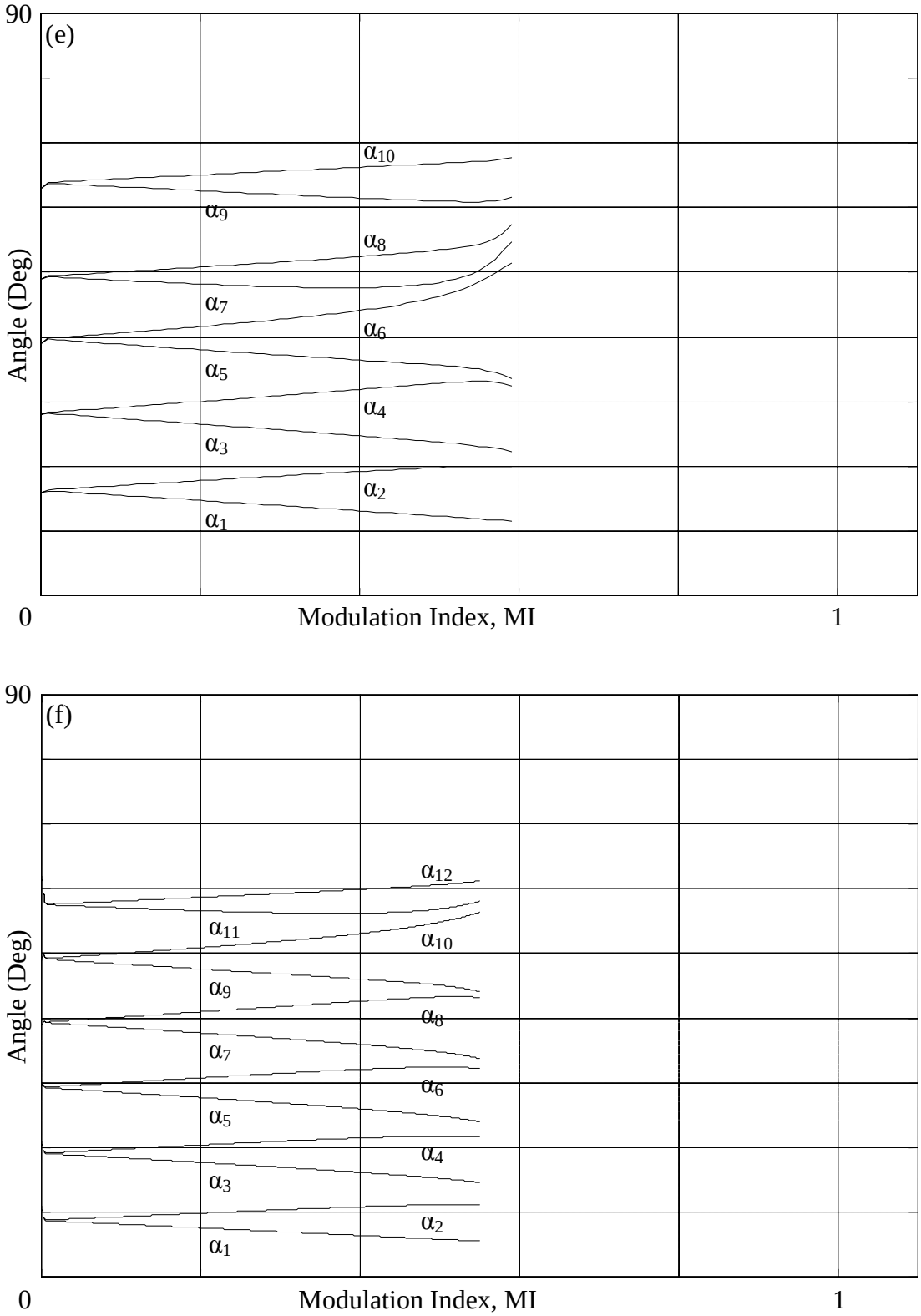

Fig. 3. Trajectories of Solutions for programmed PWM: (e) R = 10, and (f) R = 12

Fig. 3a shows that there is a linear progression of angles α_1 and α_2 following a negative or positive slope respectively in the interval $0 < MI < 0.6$.

This note is also valid for fig. 3b, fig. 3c, and fig. 3d; however in the interval 0.6 < MI < 1.1 these trajectory become non linear, thus a more refinement of the algorithm is carried out to obtain the solutions in this interval. As for fig. 3e and fig. 3f, the system has no solutions beyond MI > 0.6. We conclude from fig. 3 that maximum of the modulation index diminish with the increase of the harmonics number eliminated illustrated. For some values of R, the trajectories of the angles get nearer which implies a decrease in the width of pulses [3].

3. Simulation results using PSpice

In order to check the validity of the calculated results of the angles, the three-phase inverter system connected to a load is modelled using PSpice.

The modelling of the switch is a simple version. It consists of an infinite value of a resistance for the open state and a low value resistance for the close state. Fig.4 represents this principle.

In order to model the inverter system by PSpice, fig. 1 schematic is used with resistive load.

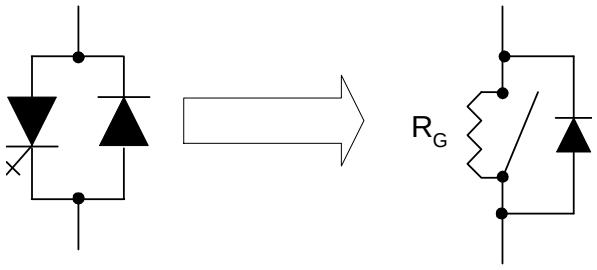

Fig. 4. Simplified model of the switch with its anti-parallel diode by PSpice

On the basis of the Pspice program various simulations have been undertaken. Fig.5 illustrates the results for the case: R = 2 and MI = 0.8, fig. 5a represents the line voltage and fig. 5b its harmonics spectra.

We notice the total elimination of harmonic of order 5.

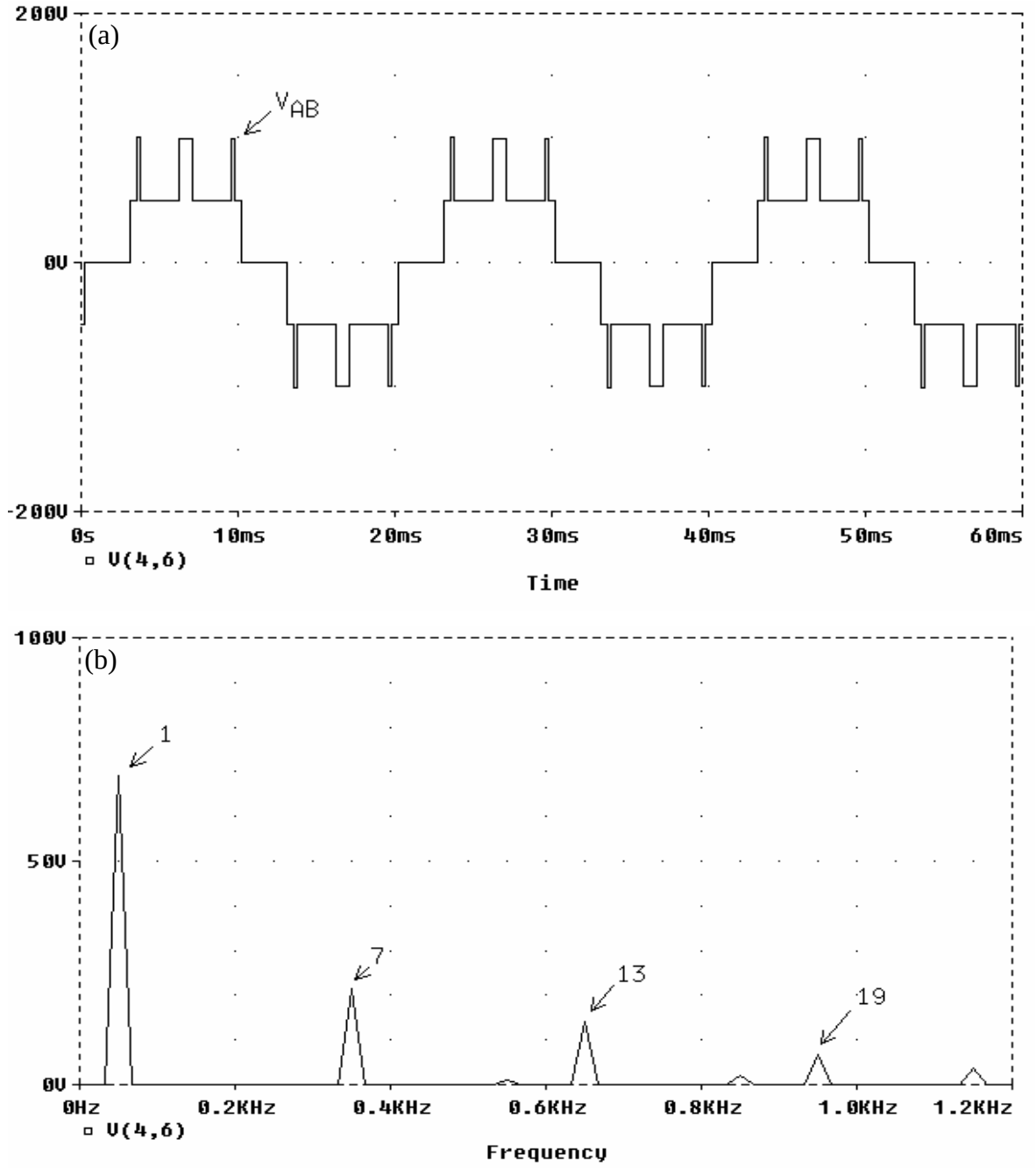

Fig. 5. Simulation results for MI = 0.8 and R = 2
(a) Line voltage, (b) Harmonics spectra; THD =31.36%

4. Application harmonics elimination method

We used the harmonics elimination method described bellow to control the static VAR compensator (ASVC) which uses a three level converter of voltage source type as shown in

fig. 6. The operating principles of the system can be explained by considering the per-phase fundamental equivalent circuit of the ASVC system as shown in fig. 7.

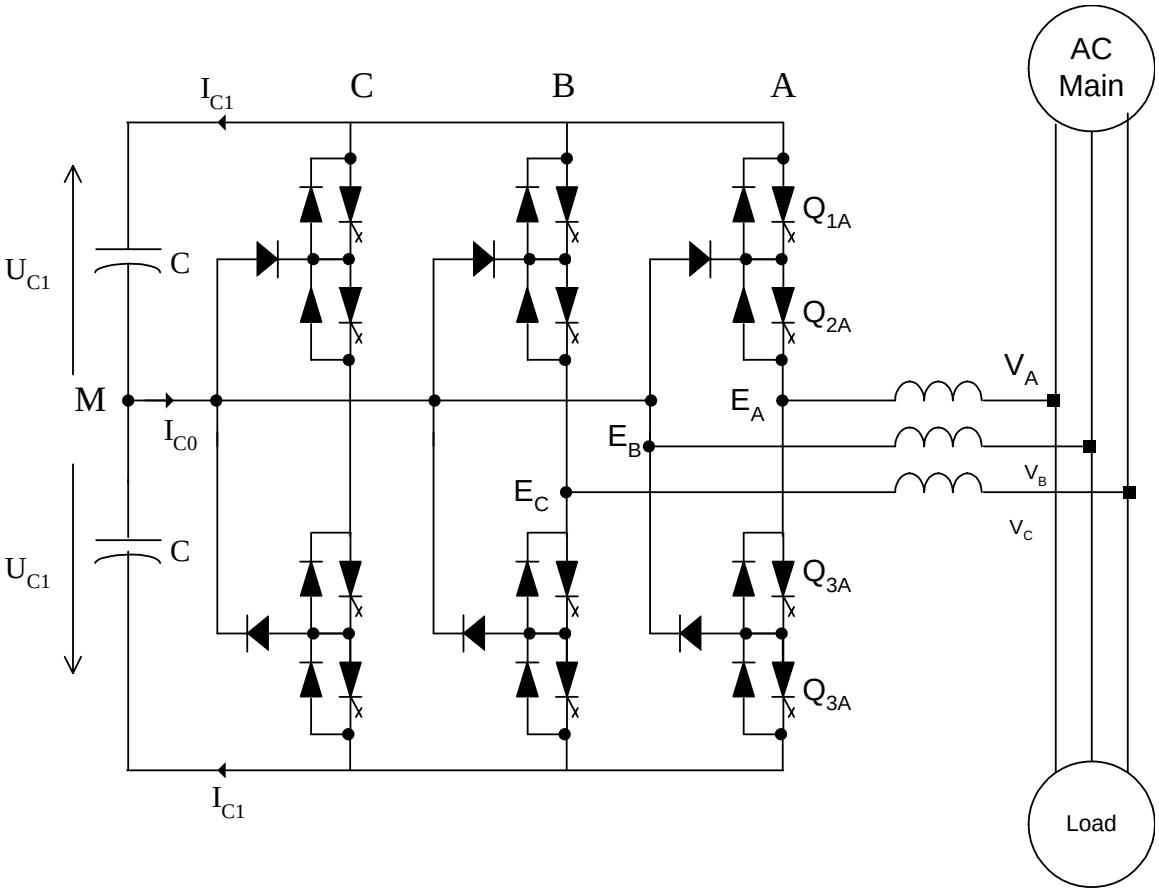

Fig. 6. Power Circuit of the ASVC

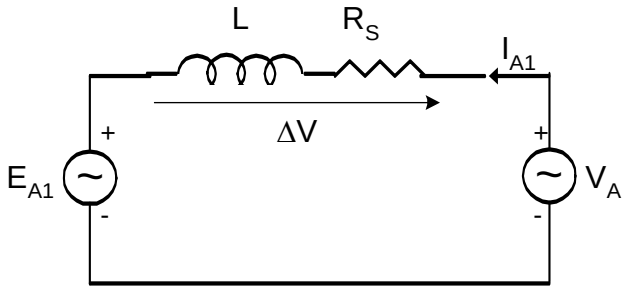

Fig. 7. Per-phase fundamental equivalent circuit

In this figure, E_{A1} is the ac mains voltage source. I_{A1} and V_A are the fundamental components of the output current and voltage of the inverter supply respectively.

The ASVC is connected to the ac mains through a reactor Ls and a resistor *R* representing the total loss in the inverter.

Reactive power control method

As shown in fig. 8, by controlling the phase angle 'α' of the inverter output voltage, the DC capacitor voltage U_C can be changed. Thus, the amplitude of the fundamental component E_{A1} can by controlled. In order to synthesize the control strategy of the system, the analysis is carried out using (dq) axis [3]. To achieve fast dynamic response it is required that by controlling the phase angle changes the capacitors Uc1 and Uc2 'α' will change. Small signal equivalent model system is used to calculate the transfer function of the system. The ASVC control scheme is illustrated in the block diagram of fig. 9. The design of the PI controller is described in [14].

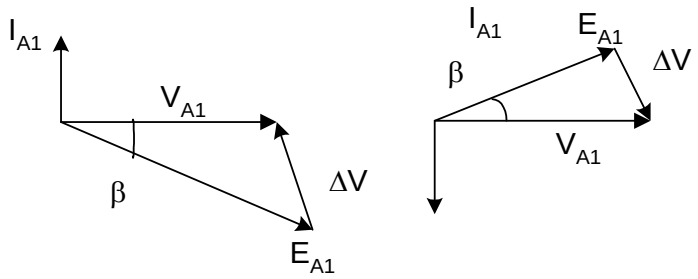

Fig. 8. Phasor Diagram for leading and lagging mode

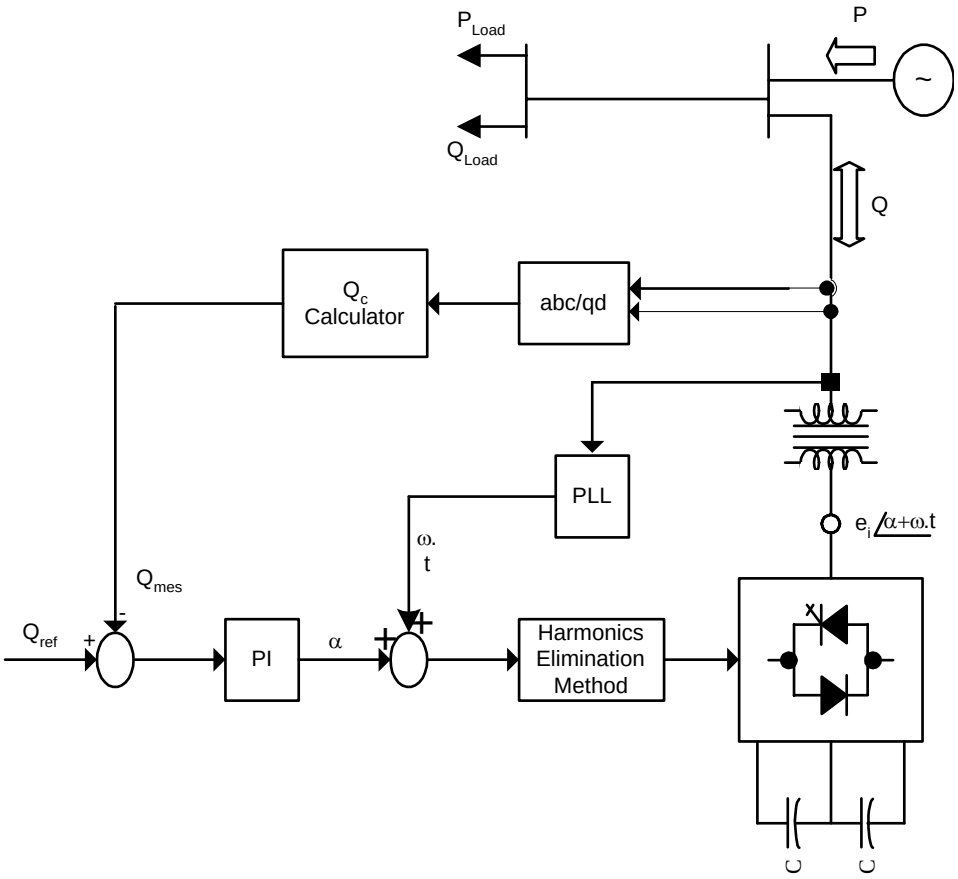

Fig. 9. Main circuit and control block diagram

Simulation results

To check the validity of the model described above a set of simulation tests have been carried out to analyse the system under steady state and transient conditions. Computer simulation is carried out using the system parameters given by: f = 60 [Hz], W = 2πf, Vs = 550 [V], Rs = 0.4 [Ω], L = 10 [mH], C = 1000 [μF], MI (modulation index) = 1, and R = 4, α_1 = 15°, α_2 = 64°, α_3 = 78°, α_4 = 84°.

Based on the linear model described in [13] and using root locus technique the parameters of the controller are found to be:

Kp = 10^{-5}, Ki = $1.8 \cdot 10^{-4}$.

The amplitude of the reference was adjusted to cause the system to swing from lagging mode to leading mode. Fig. 10 shows the simulated current and voltage waveforms to step reference of reactive power.

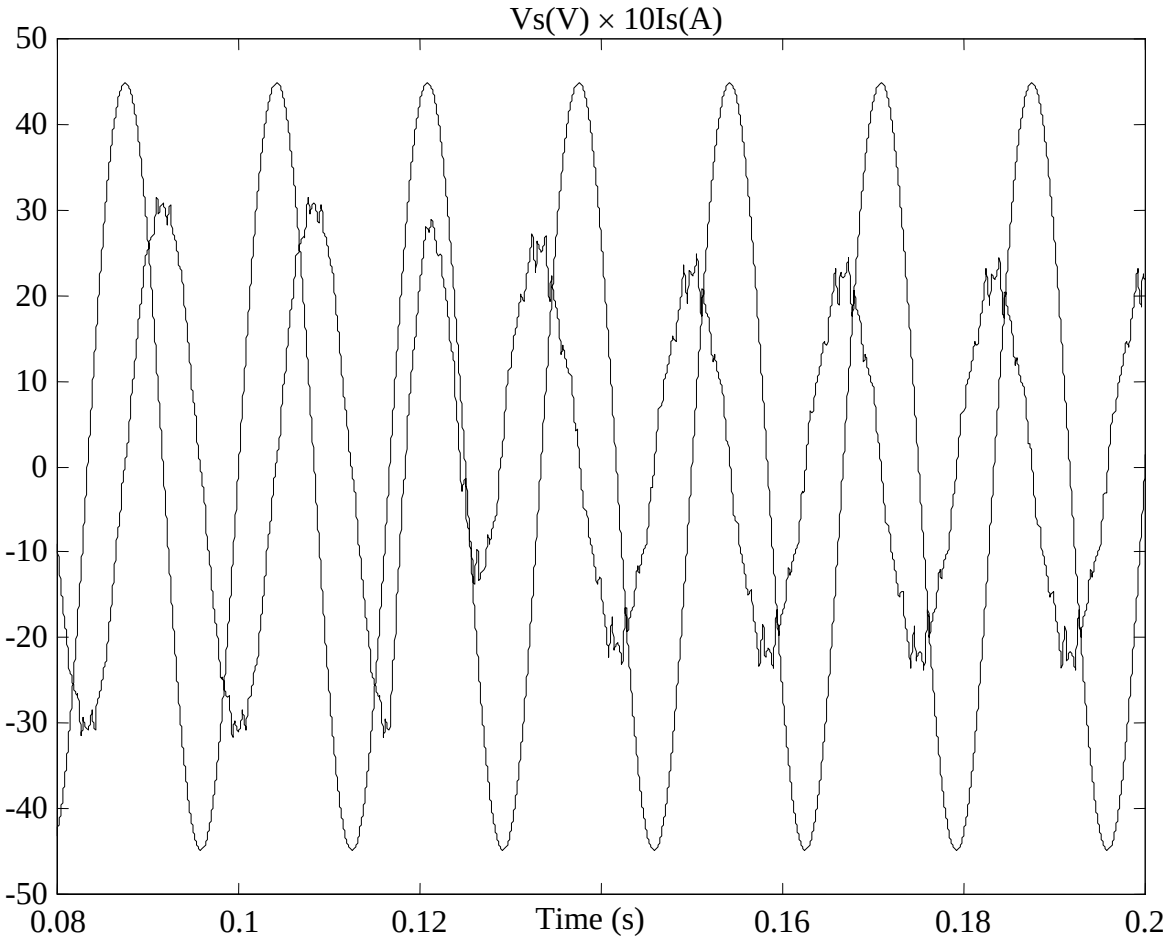

Fig. 10. Simulated current and voltage waveforms

Fig. 11 represents the current in lagging and leading mode and ther harmonics spectra respectively. We notice an increase of the amplitude of harmonics in leading mode with respect to lagging mode. This effect is caused by the DC capacitors voltage fluctuation.

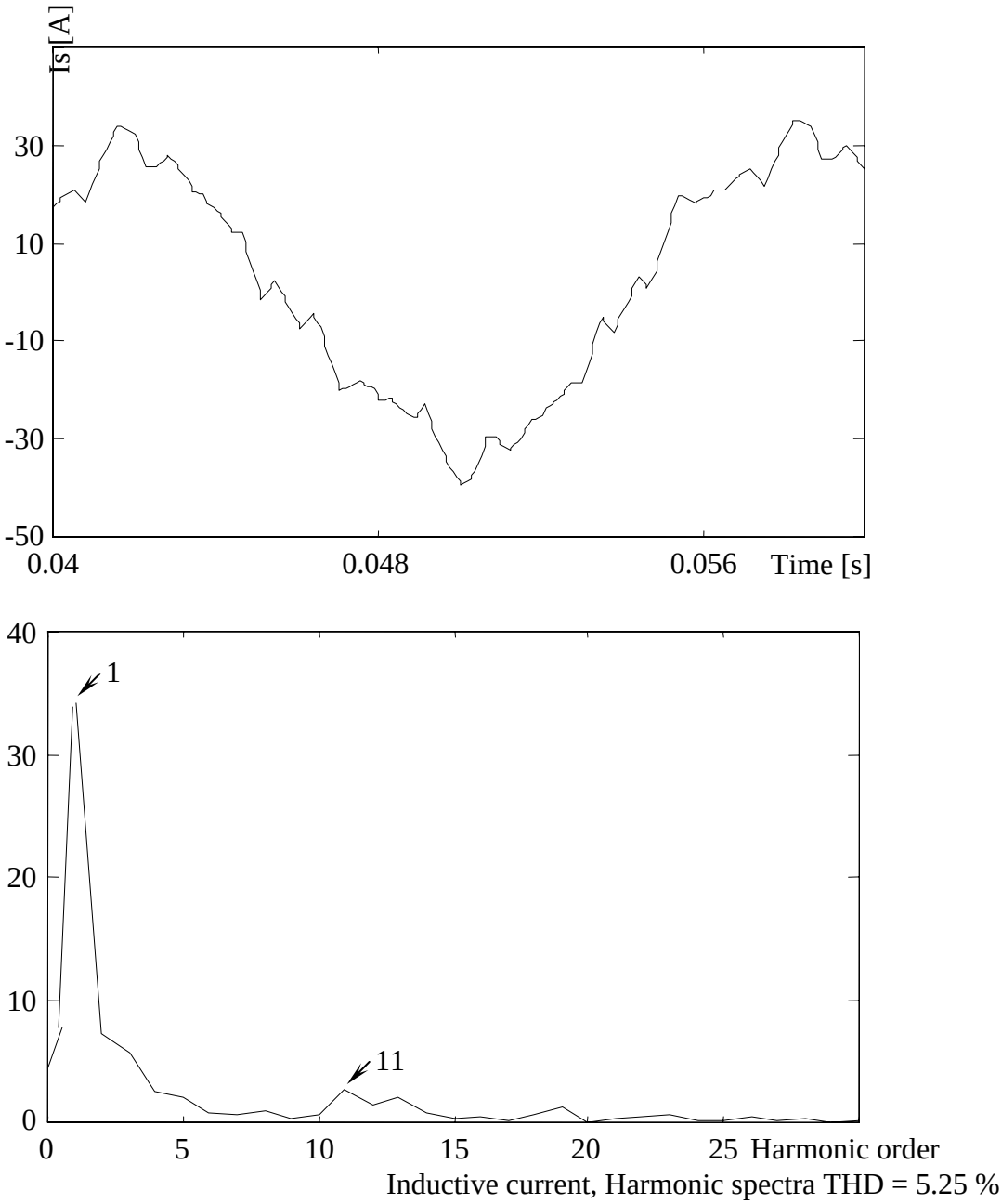

Fig. 11. Currents and harmonic spectrum (a) leading mode

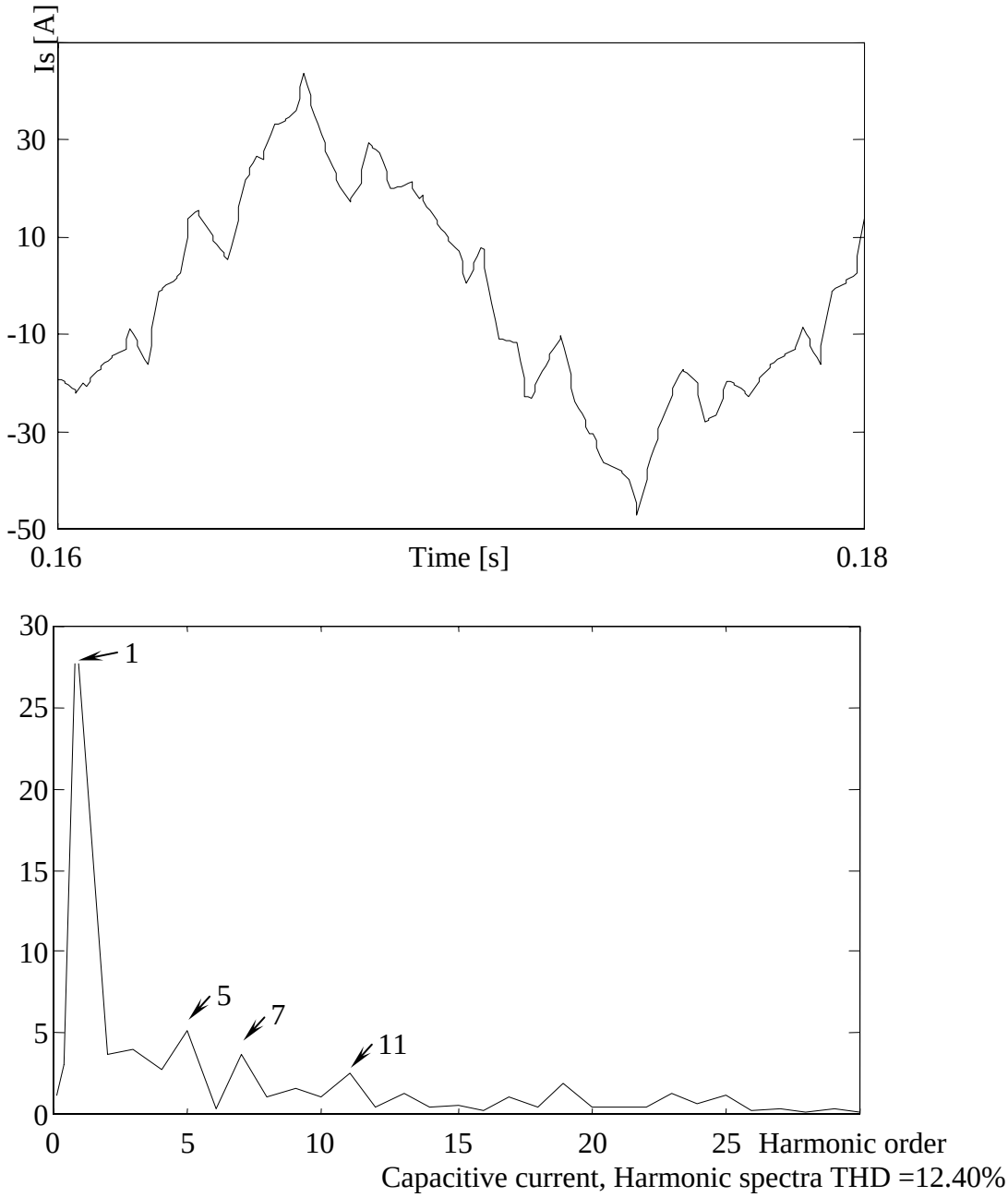

Fig. 11. Currents and harmonic spectrum (b) lagging mode

Conclusions

The main conclusion results are summarised below:

- The resolution of the non-linear equations in the case of three level inverter must be carried out with a refinement of the calculation step beyond MI>0.6 so to obtain a finite solution;

- The increase in the harmonics number eliminated has a negative effect on the modulation index since with the increase of R a decrease in MI maximum follows;
- The trajectories getting nearer for MI > 0.6 implies the decrease of the switching pulses of the GTO's which itself allows for the increase in commutation losses;

The use of a three level inverter for the ASVC allows an increase of power use and voltage waveforms quality, certainly but we note that:

- The behaviour of the system depends on the operating mode;
- The DC voltage fluctuations cause apparition of eliminated harmonics.

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